B13 include an interrupt generator for generating an interrupt to the communications processor along the bus.

REMARKS

Claims 1-27, 29-32, 34-38 and 40-42 remain in this application. Claims 28, 33 and 39 have been cancelled. Claims 1, 5, 7, 10, 16, 17, 19, 24, 27, 31, 32, 36, 38 and 42 have been amended. New Claims 43, 44 and 45 have been added.

Applicant thanks the Examiner for the detailed study of this application and the prior art.

At the outset, Applicant has added new Claims 43, 44 and 45 that are independent claims that recite the interrupt bus connected between the FIFO receive memory and communications processor such that the FIFO receive memory includes an interrupt generator for generating an interrupt through the communications processor along the bus. This subject matter had been previously indicated as allowable by the Examiner and that recitation has been added into respective claims for the system that corresponded to previous independent Claims 27 and 32 and the network controller (Claim 38).

Applicant also thanks the Examiner for the indication of allowed subject matter directed to issuing a command to a direct memory access unit of the network device to transfer data from the FIFO receive memory to the shared system memory after the communications processor has received the start-of-packet interrupt.

At the outset, Applicant has amended the independent claims to further define that a burst of data is transferred after receiving a start-of-packet interrupt. The Examiner had indicated allowable subject matter, but Applicant also notes that the cited U.S. Patent No. 5,691,984 to Gardner et al. (hereinafter "Gardner"), which was used to reject most claims as anticipated, does not disclose or suggest transferring any burst of data after receiving a start-of-packet interrupt as set forth in the amended claims. Column 8, starting at line 46, (used by the Examiner to reject a use of a start-of-packet interrupt), and teaches the use of an input data queue and an input mail, which contains information of the package status, package size and next address of the input queue.

As stated in Gardner:

> "FIG. 6B shows the flow chart of the processing performed on a data token if rotary buffer processing is configured by the CSI 11. When describing data structures, rotary buffers are also referred to as circular buffers. An rotary Input Data Queue (IDQ) is created in central shared memory 6 by the CSI configuring the Input Frame Steering 4 with a starting address and a size, either directly or through the use of an ending address. Each entry in the IDQ is a data frame. The IDQ is filled as data is input to the system 20a using either the AIB 5 or the dedicated Local Memory Interface. Data frames are placed in the IDQ in a contiguous fashion until the IDQ size has been exhausted. The IDQ then wraps back to the starting location and continues placing data in memory. Also, the switch port 7 sends an input mail to the central switch intelligence 11 with an input mail

> which contains the information of the packet status, packet size and the next address of the input queue. The next address of the input queue and of the input mail box is updated in the switch port 7."

There is no disclosure or any other teaching in Gardner to suggest the transfer of a burst of data after receiving a start-of-packet interrupt, where the burst of data includes the preselected address fields from the FIFO receive memory to the external shared system memory, while also generating an interrupt signal to the host processor indicative that the preselected address fields of the frame are present in the shared system memory and initiating within the host processor an address and look-up algorithm and address table to determine frame routing based on the preselected address fields.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version With Markings to Show Changes Made."**

Applicant contends that the present case is in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance and Issue Fee Due.

In re Patent Application of:
KASPER
Serial No. **09/163,925**
Filing Date: **09/30/1998**
_____/

If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,

RICHARD K. WARTHER
Reg. No. 32,180
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, WASHINGTON, DC 20231**, on this 30th day of January, 2003.

In re Patent Application of:
KASPER
Serial No. **09/163,925**
Filing Date: **09/30/1998**
_____/

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 28, 33 and 39 have been cancelled.

Claims 1, 5, 7, 10, 16, 17, 19, 24, 27, 31, 32, 36, 38 and 42 have been amended as follows:

1. (ONCE AMENDED) A method of routing network-based data arranged in frames comprising the steps of:

receiving a first portion of a frame within a FIFO receive memory of a network device, wherein the first portion of the received frame includes data having preselected address fields;

transferring a burst of data after receiving a start-of-packet interrupt, including preselected address fields, from the FIFO receive memory to an external shared system memory that exists between the network device and a host processor;

generating an interrupt signal to the host processor indicative that the preselected address fields of the frame are present in the shared system memory; and

initiating within the host processor an address and look-up algorithm in address tables to determine frame routing based on the preselected address fields.

5. (ONCE AMENDED) A method of routing according to Claim 1, and further comprising the step of receiving [the] **a** balance of the frame completely within the shared system memory.

7. (ONCE AMENDED A method of routing according to Claim 1, and further comprising the step of generating [a] the start-of-packet interrupt to a communications processor within the network device when the data received within the FIFO receive memory has reached a desired watermark value.

10. (ONCE AMENDED) A method of controlling network data flow arranged in frames comprising the steps of:

receiving at least a first portion of a frame containing data receive memory of a network device, wherein the first portion of the received frame includes data having preselected address fields;

transferring a burst of data after receiving a start-of-packet interrupt, including preselected address fields, from the FIFO receive memory to a shared system memory that exists between a host processor and the network device; and

generating an interrupt signal to the host processor indicative that the preselected address fields of the frame are present in the memory.

16. (ONCE AMENDED A method according to Claim 10, and further comprising the step of generating [a] the start-of-packet interrupt to a communications processor when the data received within the receive memory has reached a desired watermark value.

19. (ONCE AMENDED) A method of routing network-based data arranged in frames comprising the steps of:

receiving at least a first portion of a frame within a FIFO receive memory of a network device, wherein the first portion of the received frame includes data having preselected address fields;

selecting the amount of data to be transferred from the FIFO receive memory based on the desired address fields to be analyzed by a host processor;

transferring a burst of data, including preselected address fields after receiving a start-of-packet interrupt, from the FIFO receive memory to a shared system memory that exists between the network device and the host processor;

generating an interrupt signal from the network device to the host processor indicative that the preselected address fields of the frame are present in the shared system memory; and

initiating an address and look-up algorithm to determine frame routing based on the preselected address fields.

24. (ONCE AMENDED) A method of routing according to Claim 19, and further comprising the step of generating [a] the start-of-packet interrupt to a communications processor of the network device when the data received within the FIFO receive memory has reached a watermark value.

27. (ONCE AMENDED) A system for routing network-based data arranged in frames comprising:

a FIFO receive memory of a network device for receiving at least a first portion of a frame, wherein the

first portion of the frame includes data having preselected address fields;

a host processor;

a shared system memory that exists between the network device and host processor for receiving data, including the preselected address fields, from the FIFO receive memory;

a direct memory access unit for transferring a burst of data from the FIFO receive memory to the shared system memory; and

a communications processor for selecting the amount of data to be transferred from the FIFO receive memory to the shared system memory based on the desired address fields to be analyzed by the host processor <u>after receiving a start-of-packet interrupt</u>.

31. (ONCE AMENDED) A system according to Claim 27, wherein said FIFO receive memory has a watermark value, and means for issuing [a] <u>the</u> start-of-packet interrupt to the communications processor when the watermark value is reached.

32. (ONCE AMENDED) A system for routing network-based data arranged in frames comprising:

a host processor for analyzing transferred bursts of data and initiating an address and lookup algorithm for dispatching a frame to a desired destination;

a shared memory for receiving data, including any preselected address fields; and

a network device having:

a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the receive memory to the shared system memory; and

a communications processor for selecting the amount of data to be transferred from the receive memory based on the desired address fields to be analyzed by the host processor <u>after receiving a start-of-packet interrupt</u>.

36. (TWICE AMENDED) A system according to Claim 32, wherein said receive memory has a watermark setting at which the [HDLC] port issues [a] <u>the</u> start-of-packet interrupt to the communications processor.

38. (ONCE AMENDED) A network controller having:

a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the FIFO receive memory to an external system memory jointly shared with a host; and

a communications processor for selecting the amount of data to be transferred from the FIFO receive memory based

on the desired address fields to be analyzed by a host processor after receiving a start-of-packet interrupt.

42. (ONCE AMENDED) A network controller according to Claim 38, wherein said receive memory has a watermark setting at which the port issues [a] the start-of-packet interrupt to the communications processor.

New Claims 43, 44 and 45 are added as follows:

43. A system for routing network-based data arranged in frames comprising:

a FIFO receive memory of a network device for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a host processor;

a shared system memory that exists between the network device and host processor for receiving data, including the preselected address fields, from the FIFO receive memory;

a direct memory access unit for transferring a burst of data from the FIFO receive memory to the shared system memory;

a communications processor for selecting the amount of data to be transferred from the FIFO receive memory to the shared system memory based on the desired address fields to be analyzed by the host processor; and

an interrupt bus connected between the FIFO receive memory and communications processor, wherein said FIFO receive memory includes an interrupt generator for generating an interrupt to the communications processor along the bus.

44. A system for routing network-based data arranged in frames comprising:

a host processor for analyzing transferred bursts of data and initiating an address and lookup algorithm for dispatching a frame to a desired destination;

a shared memory for receiving data, including any preselected address fields; and

a network device having:

a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the receive memory to the shared system memory;

a communications processor for selecting the amount of data to be transferred from the receive memory based on the desired address fields to be analyzed by the host processor; and

an interrupt bus connected between the FIFO receive memory and communications processor, wherein said ports include an interrupt generator for generating an interrupt to the communications processor along the bus.

45. A network controller having:

a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the FIFO receive memory to an external system memory jointly shared with a host;

a communications processor for selecting the amount of data to be transferred from the FIFO receive memory based on the desired address fields to be analyzed by a host processor; and

an interrupt bus connected between the FIFO receive memory and communications processor, wherein said ports include an interrupt generator for generating an interrupt to the communications processor along the bus.